CLAIMS

What is claimed is:

1. A system using a current controlled charging circuit for charging columns of a liquid crystal display, said system comprising:

a liquid crystal display (LCD) having a matrix of liquid crystal pixels, said matrix comprising a plurality of columns and a plurality of rows, wherein an intersection of a row and a column defines a location of a pixel; and

at least one digital-to-analog converter (DAC) adapted to receive digital inputs representative of pixel gray scales, said at least one DAC having an output adapted for charging each of said plurality of columns to voltages representing said pixel gray scales, wherein the output comprises current source pulses having amplitudes and pulse-widths that charge each of said plurality of columns to said voltages.

2. The system of claim 1, wherein a plurality of row switches selectively couples said matrix of pixels to said plurality of columns.

3. The system of claim 2, wherein a plurality of column switches selectively couples the output of said at least one DAC to each of said plurality of columns.

4. The system of claim 3, wherein column control logic controls said plurality of column switches and row control logic controls said plurality of row switches.

5. The system of claim 4, further comprising an LCD pixel matrix address controller adapted for controlling said column and row control logic.

6. The system of claim 5, further comprising a video frame to LCD pixel matrix address logic coupled to said LCD pixel matrix address controller, said video frame to LCD pixel matrix address logic adapted to receive video information and generate LCD pixel matrix addresses for said LCD pixel matrix address controller.

7. The system of claim 1, further comprising a gray scale current pulse look-up table adapted for converting said pixel gray scales into the digital inputs received by said at least one DAC.

8. The system of claim 7, further comprising a gray scale conversion logic coupled to said gray scale current pulse look-up table.

9. The system of claim 8, wherein said gray scale conversion logic is adapted to receive video information and generate said pixel gray scales for said gray scale conversion logic.

10. The system of claim 1, further comprising a pulse-width time control circuit for controlling the pulse-widths of said current source pulses.

11. The system of claim 10, wherein said pulse-width time control circuit is coupled to a gray scale current pulse look-up table.

12. The system of claim 10, wherein said pulse-width time control circuit is synchronized with a column clock.

13. The system of claim 12, further comprising a phase-locked-loop (PLL) coupled between the column clock and a clock input to said pulse-width time control circuit, wherein said PLL is adapted to synchronize said clock input with said column clock.

14. The system of claim 13, wherein said PLL generates said clock input to said pulse-width time control circuit.

15. The system of claim 1, further comprising an analog-to-digital converter (ADC) for converting said voltages on said columns to digital voltage values.

16. The system of claim 15, further comprising a digital comparator for comparing said voltages representing said pixel gray scales with said digital voltage values from said ADC.

17. The system of claim 16, wherein comparisons of said voltages representing said pixel gray scales with said digital voltage values are used in determining compensation coefficients for each of said plurality of columns having different capacitance values.

18. The system of claim 17, further comprising a memory for storing said compensation coefficients.

19. The system of claim 1, wherein each of said plurality of columns has substantially the same capacitance.

20. The system of claim 1, wherein each of said plurality of columns is compensated to have substantially the same capacitance.

21. The system of claim 20, further comprising at least one capacitor connected to some ones of said plurality of columns such that each of said plurality of columns has substantially the same capacitance as another column.

22. The system of claim 21, further comprising a column capacitance compensation circuit and at least one switch for coupling said at least one capacitor to said some ones of said plurality of columns.

23. The system of claim 22, further comprising a column capacitance compensation memory coupled to said column capacitance compensation circuit, said column capacitance compensation memory storing connection setting for said at least one switch for coupling said at least one capacitor to said some ones of said plurality of columns.

24. The system of claim 21, wherein said at least one capacitor is a plurality of capacitors having capacitance values in a binary progression.

25. The system of claim 1, wherein said LCD is fabricated on a semiconductor integrated circuit.

26. The system of claim 25, wherein said at least one DAC is fabricated on said semiconductor integrated circuit.

27. The system of claim 3, wherein said plurality of column switches and said plurality of row switches are fabricated on a semiconductor integrated circuit.

28. The system of claim 4, wherein said column control logic and said row control logic are fabricated on a semiconductor integrated circuit.

29. The system of claim 5, wherein said LCD pixel matrix address controller is fabricated on a semiconductor integrated circuit.

30. The system of claim 6, wherein said video frame to LCD pixel matrix address logic is fabricated on a semiconductor integrated circuit.

31. The system of claim 7, wherein said gray scale current pulse look-up table is fabricated on a semiconductor integrated circuit.

32. The system of claim 8, wherein said gray scale conversion logic is fabricated on a semiconductor integrated circuit.

33. The system of claim 10, wherein said pulse-width time control circuit is fabricated on a semiconductor integrated circuit.

34. The system of claim 11, wherein said gray scale current pulse look-up table is fabricated on a semiconductor integrated circuit.

35. The system of claim 16, wherein said comparator and said ADC are fabricated on a semiconductor integrated circuit.

36. The system of claim 22, wherein said column capacitance compensation circuit and said at least one switch are fabricated on a semiconductor integrated circuit.

37. A current controlled charging circuit adapted for charging columns of a liquid crystal display having a matrix of liquid crystal pixels, said current controlled charging circuit comprising:

at least one digital-to-analog converter (DAC) adapted to receive digital inputs representative of pixel gray scales, said at least one DAC having an output adapted for charging each of a plurality of columns of a liquid crystal display (LCD) to voltages representing said pixel gray scales, wherein the output comprises current source pulses having amplitudes and pulse-widths that charge each of said plurality of columns to said voltages.

38. The current controlled charging circuit of claim 37, further comprising a gray scale current pulse look-up table adapted for converting said pixel gray scales into the digital inputs received by said at least one DAC.

39. The current controlled charging circuit of claim 38, further comprising a gray scale conversion logic coupled to said gray scale current pulse look-up table.

40. The current controlled charging circuit of claim 39, wherein said gray scale conversion logic is adapted to receive video information and generate said pixel gray scales for said gray scale conversion logic.

41. The current controlled charging circuit of claim 37, further comprising a pulse-width time control circuit for controlling the pulse-widths of said current source pulses.

42. The current controlled charging circuit of claim 41, wherein said pulse-width time control circuit is coupled to a gray scale current pulse look-up table.

43. The current controlled charging circuit of claim 41, wherein said pulse-width time control circuit is synchronized with a column clock.

44. The current controlled charging circuit of claim 43, further comprising a phase-locked-loop (PLL) coupled between the column clock and a clock input to said pulse-width time control circuit, wherein said PLL is adapted to synchronize said clock input with said column clock.

45. The current controlled charging circuit of claim 44, wherein said PLL generates said clock input to said pulse-width time control circuit.

46. The current controlled charging circuit of claim 37, further comprising a comparator circuit for comparing said voltages representing said pixel gray scales with said voltages from said ADC.

47. The current controlled charging circuit of claim 46, wherein comparisons of said voltages representing said pixel gray scales with said voltage are used in determining compensation coefficients for each of said plurality of columns having different capacitance values.

48. The current controlled charging circuit of claim 47, further comprising a memory for storing said compensation coefficients.

49. A method using a current controlled charging circuit for charging columns of a liquid crystal display, said method comprising the steps of:

providing a liquid crystal display (LCD) having a matrix of liquid crystal pixels, said matrix comprising a plurality of columns and a plurality of rows, wherein an intersection of a row and a column defines a location of a pixel; and

charging with a current controlled charging circuit each of said plurality of columns to voltages representing pixel gray scales.

50. The method of claim 49, wherein the current controlled charging circuit is a current output digital-to-analog converter (DAC).

51. The method of claim 49, further comprising the step of selectively coupling said matrix of pixels to said plurality of columns.

52. The method of claim 49, wherein the step of charging is done with current pulses.

53. The method of claim 52, further comprising the step of controlling amplitudes of said current pulses.

54. The method of claim 52, further comprising the step of controlling pulse-widths of said current pulses.

55. The method of claim 54, wherein the pulse-widths are determined with a gray scale current pulse look-up table.

56. The method of claim 49, further comprising the step of measuring the voltages on said plurality of columns.

57. The method of claim 56, further comprising the step of comparing the voltages representing the pixel gray scales with the voltages measured on said plurality of columns.

58. The method of claim 57, further comprising the step of determining compensation coefficients from differences between the voltages representing the pixel gray scales and the voltages measured on said plurality of columns for each of said plurality of columns.

59. The method of claim 58, further comprising the step of storing the compensation coefficients in a memory.

60. The method of claim 49, further comprising the step of adding compensating capacitance to said plurality of columns such that each of said plurality of columns has substantially the same capacitance as the others.

61. The system of claim 1, further comprising a circuit for setting said plurality of columns to a desired voltage before charging said plurality of columns to said voltages.

62. The system of claim 61, wherein the desired voltage is substantially zero.

63. The system of claim 1, further comprising a circuit for discharging said plurality of columns before charging said plurality of columns to said voltages.

64. The system of claim 1, further comprising a comparison circuit for comparing said voltages representing said pixel gray scales with said voltages on said columns, said comparison circuit output being used in determining compensation coefficients for each of said plurality of columns having different capacitance values.

65. The system of claim 20, wherein each of said plurality of columns is compensated with a fuse link connected plurality of capacitors.

66. The method of claim 60, wherein the step of adding compensating capacitance to said plurality of columns comprises the steps of blowing fuse links connected to a plurality of compensation capacitors.